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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,230	08/30/2001	John Whitman	4294.1US (98-1208.1)	2488

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/944,230	Applicant(s) WHITMAN ET AL.	
	Examiner Thomas L Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *2 and 5-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,11-13 and 15-24* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *13 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/30/2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 23,24, and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by YATES et al. (6,358,793).

Yates et al. discloses a semiconductor device structure with a substantially planar surface, comprising a substrate 5-10-15 including at least one recess (no #; it is the recess that is partially filled by part 90) formed therein, and a material layer 90 disposed at least partially over the substrate 5-10-15 and at least one intermediate layer 20, comprising at least one of a mask material, an insulative material, and a conductive material, namely, conductive HSG silicon, between the substrate 5-10-15 and the material layer 90, so that the material layer 90 and the at least one intermediate layer 20 each at least partially fill the at least one recess, wherein the surface of the material layer 90 is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys; and where at least one region of the at least one intermediate layer 20 and at least one region of the substrate 5-10-15 is exposed through the material layer 90, and the material layer 90 has a thickness that is less than a depth of the at least one recess. Note figures 11, 12, 7, and column 10 lines 1-31of Yates et al.

B. Claims 21,22,1,3, and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by KIKUCHI ET AL. (6,278,153).

Kikuchi et al. discloses a semiconductor device structure with a substrate 21-22-23-24-25-26 including at least one recess 23A formed therein, and a material layer 20 disposed over the substrate 21-22-23-24-25-26 and substantially filling the at least one recess 23A, wherein the surface of the material layer 20 is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and

valleys; and wherein the substrate 21-22-23-24-25-26 comprises a stacked capacitor structure 22-23-24-25-26 and the at least one recess 23A comprises at least one container 27 recessed in an insulator layer 23 of the stacked capacitor structure 22-23-24-25-26. Note figures 6B, 6F and column 19 lines 35-67 and column 20 lines 13-27 of Kikuchi et al.

With special regard to claims 3,12, and 13, Kikuchi et al. discloses that the material layer 20 comprises a mask material (note column 20 lines 14-17), the mask material substantially filling the at least one container 27, wherein the mask material has a thickness of (note the thickness disclosed by figure 6F) less than a depth of the at least one container 27.

C. Claims 21,22,1,23,24,15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by WANG (6,461,932), cited by the applicant on 11/03/03.

Wang discloses a semiconductor device structure with a substantially planar surface, comprising a substrate 40 including at least one recess 54 formed therein; and a material layer 56A disposed over said substrate 40 and substantially filling said at least one recess 54, so as to at least partially fill said at least one recess 54, wherein at least one region of said substrate 40 is exposed through said material layer 56A, and wherein the surface of said material layer 56A is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys. Note figure 4F and column 6 lines 23-51 and column 8 lines 26-39 of Wang.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over KIKUCHI et al. (6,278,153) in view of DENNISON et al. (5,663,090).

Kikuchi et al. discloses a semiconductor device structure with all the limitations of claim 4 except that the substrate include at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess. Note figure 6F of Kikuchi et al.

However, Dennison et al. discloses a semiconductor device structure with substrate 40 including at least one conductively doped region 41 that is adjacent to a recess (the recess being filled with lower electrode 43 of a stacked capacitor structure. Note figure 4b of Dennison et al. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of Kikuchi et al.'s semiconductor device structure with the substrate including at least one conductively doped region that is adjacent a recess containing a stacked capacitor structure, such as taught by Dennison et al. in order to utilize the semiconductor device structure of Kikuchi et al. alongside a MOSFET such as

taught by Dennison et al. to thus utilize the semiconductor device structure of Kikuchi et al. as the capacitor of a DRAM memory.

Allowable Subject Matter

3. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1,3,4,11-13, and 15-20 have been considered but are moot in view of the new ground(s) (new art and/or new reasoning applied to old art) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
04/04

Minhloan Tran
Primary Examiner
Art Unit 2826